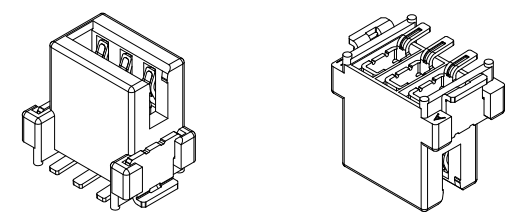
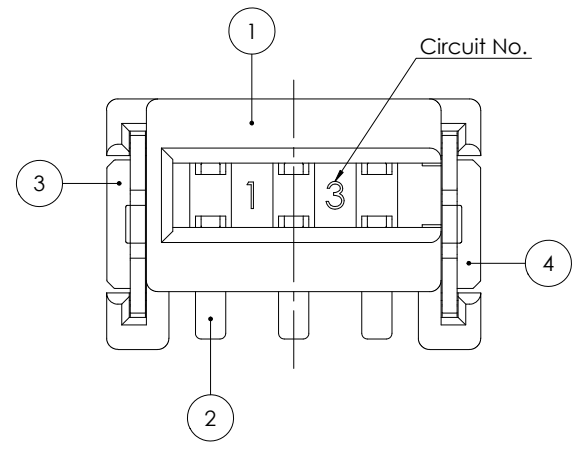
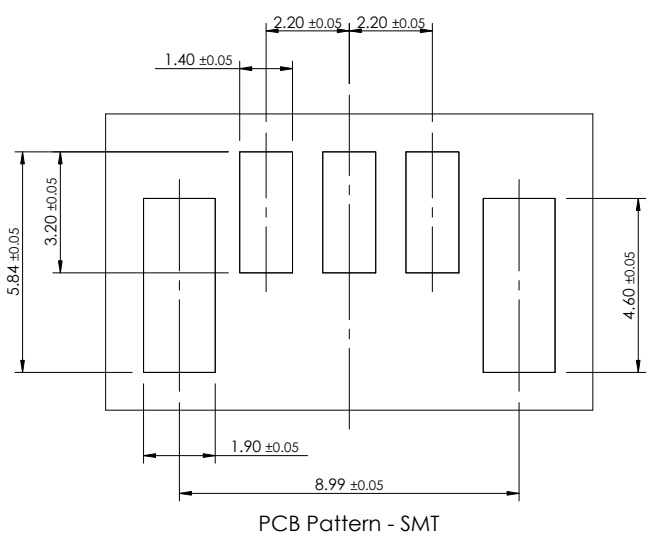
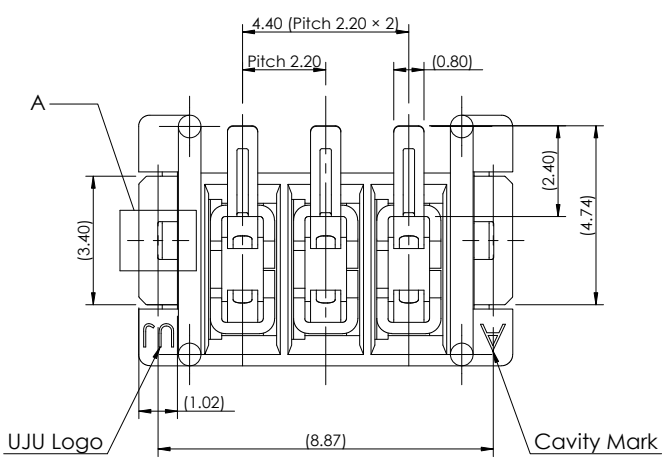
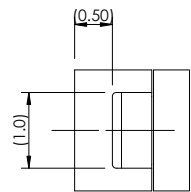
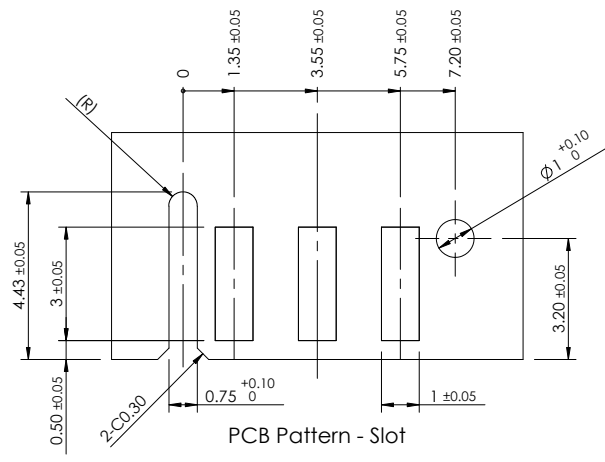
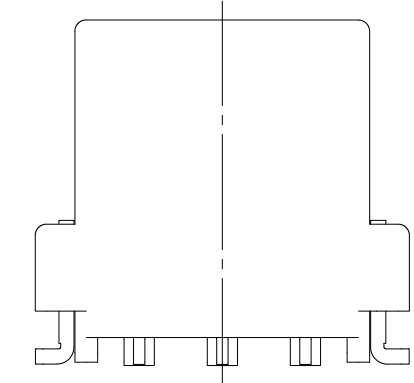
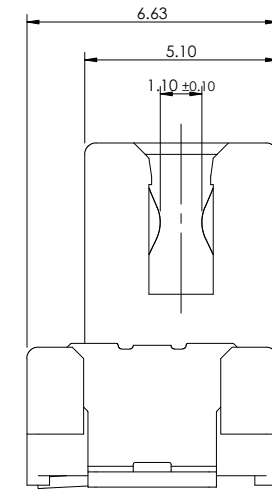
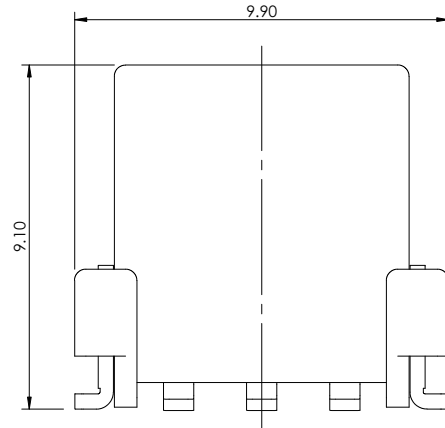
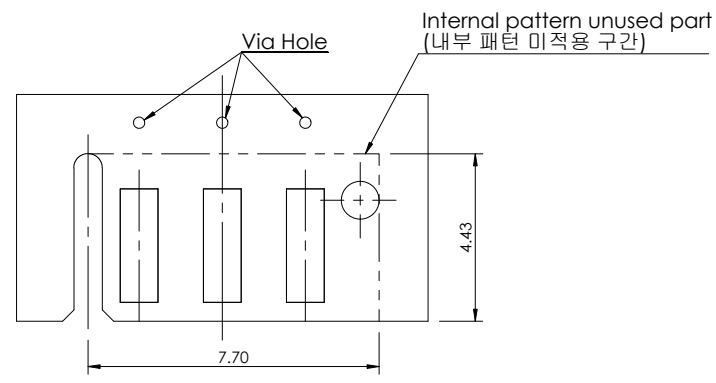


REV	REVISION RECORD	DATE	DRWN	CHKD	APVD
A	RELEASED	20 MAR '19	JK	SH	CY



3D View

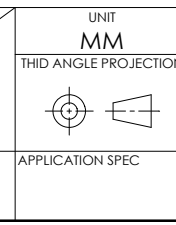


- Note. 1-
1. General Tolerance : ± 0.30
 2. Burr side is not permitted.
 3. No crack

No.	Description	Material	Finish / Color	Q'ty
4	020 S SMT Solder Peg VTC-R	Copper Alloy	Post-Tin	1
3	020 S SMT Solder Peg VTC-L	Copper Alloy	Post-Tin	1
2	PCB_Slot_SMT_F_V_TML	Copper Alloy	Post-Au/Tin	3
1	PCB_Slot_SMT_3F_V_HSG	PA9T-GF30	Black	1

- ③ -Note. 2 (PCB Pattern - Slot)-
1. Thickness : 1.60 ± 0.10
 2. Finish : Same as terminal plating
Ex) Sn/HASL \leftrightarrow Sn, Au \leftrightarrow Au
 3. Recommendation : Apply a via hole for connect both sides.
 4. Concrete specifications are discussed with UJU.

TOLERANCES UNLESS OTHERWISE SPECIFIED	UNIT MM
0	\pm
0.0	\pm
0.00	\pm
0.000	\pm
0.0000	\pm
ANGLES	\pm
PRODUCT SPEC	APPLICATION SPEC



DRWN JK. HWANG	 (주)우주일렉트로닉스 UJU Electronics co.,Ltd.	NAME	PCB_Slot_SMT_3F_V_ASSY_Au			
CHKD SH. LEE		CUSTOMER DRAWING	KH1700033			
APVD CY. CHOI		LOC	RESTRICTED TO	SIZE A3	SCALE 5:1	SHEET 1 of 1